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EXAMINER	
KIM, SU C	

ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/796,514	SNYDER ET AL.	
	Examiner	Art Unit	
	Su C. Kim	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-21,23-31 and 33-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-21,23-31 and 33-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3,5-11, 13,14,33-38, & 40-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Hossain et al. (US 6242785).

The rejections that set forth in the office action that was mailed on 9/19/2006 is maintained and repeated herein below as record.

Pertaining claim 1, Hossain discloses a method for manufacturing of a device for regulating the flow of electrical current, the method comprising;

provide for a semiconductor substrate(Fig. 1, 10);

providing for an electrical insulating layer in contact with the semiconductor substrate having a dielectric constant greater than 4.0 (Fig. 10, silicon oxynitride 12 has dielectric constant from 3.8 to 7.5 depended on content of oxygen and nitrogen)

providing for a gate electrode (Fig. 12, 38 source and drain electrode) in contact with at least with the semiconductor substrate and proximal to the gate electrode(Fig. 12, 14) wherein at least one of the source electrode and the drain electrode (Fig. 12, source and drain 30) forms a Schottky contact or Schottky-like region(Fig. 9-13, column

9 lines 20-45, a metal layer (40) selected from platinum tungsten tantalum palladium or nickel and silicided on source and drain to form electrodes) with the semiconductor substrate(Fig. 12, 38)

Pertaining claim 2, as applied to claim 1 above, Hossain discloses all the limitations include, the metal layer is silicided and metal layer is selected form platinum tungsten tantalum palladium or nickel and silicided on source and drain to form electrodes(Column 9, lines 20-45)

Pertaining claim 3, as applied to claim 1 above, Hossain discloses all the limitations include, source and drain electrodes are formed from rare earth silicides (Column 9, lines 20-45, rare earth material tantalum palladium platinum)

Pertaining claim 5, as applied to claim 1 above, Hossain discloses all the limitations include, the insulation layer is formed from an oxy-nitride stack (column 6 lines 51-53, silicon oxynitride 12 is considered as oxide-nitride stack because oxide layer is formed between the nitride and the substrate).

Pertaining claim 6, as applied to claim 1 above, Hossain discloses all the limitations include, the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel (Fig.11, 46)

Pertaining claim 7, as applied to claim 1 above, Hossain discloses all the limitations include, an entire interface between a least on of the source and drain electrode and the semiconductor substrate froms a Schottky contact or Schottky-like region with the semiconductor substrate.(Fig. 11, silicide layer 46 covers all source and drain region 30)

Pertaining claim 8, as applied to claim 1 above, Hossain discloses all the limitations include, dopant are introduced into the channel region (Fig. 1, 18)

Pertaining claim 9, as applied to claim 1 above, Hossain discloses all the limitations include, include, the insulation layer is more than one layer (Fig. 13, 12)

Pertaining claim 11, as applied to claim 2 or 3 above, Hossain discloses all the limitations include, the insulation layer is formed from an oxy-nitride stack (column 6 lines 51-53, silicon oxynitride 12 is considered as oxide-nitride stack because oxide layer is formed between the nitride and the substrate).

Pertaining claim 14, as applied to claim 2 or 3, Hossain discloses all the limitations include, providing a source electrode and a drain electrode in contact with semiconductor substrate is performed at a processing temperature of less than about 800 °C(Column 9, lines 29-31 "thermal process includes heating substrate to a temperature greater than 600 °C").

Pertaining claim 13, as applied to claim 10 above, Hossain discloses all the limitations include, The Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel (Fig. 10, 46), and wherein dopant are introduced into the channel region(Fig. 1, 18)

Pertaining claim 33, Hossian discloses a method for manufacture of device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate(Fig. 1, 10);

providing for an electrically insulating layer in contact with the semiconductor substrate the insulating layer having a dielectric constant greater than 4.0(Fig. 6, silicon oxynitride 12 having dielectric constant from 3.5 to 7.5)

providing for a gate electrode located in contact with at least a portion of the insulating layer(Fig. 6, 12)

exposing the semiconductor substrate one or more areas proximal to the gate electrode(Fig. 6, source and drain region have been exposed by etching gate insulating layer 12);

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate(Fig. 10, 40);

reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate(Fig. 13, 46).

Pertaining claim 34, as applied to claim 33 above, Hossian discloses all the limitations include, depositing a thin conducting film on the insulating layer;

patterning and etching the conducting film to form a gate electrode (Fig. 1, 14);

and forming one or more thin insulating layers (Fig.1, 12) on one or more sidewalls of the gate electrode(Fig.3, 22).

Pertaining claim 35, as applied to claim 33 above, Hossian discloses all the limitations include, removing metal not reacted during the reacting process (Fig 9-11 metal layer 40 is removed on the sidewall spacer 22)

Pertaining claim 36, as applied to claim 33 above, Hossian discloses all the limitations include, thermal annealing (Fig. 10, thermal process 42)

Pertaining claim 37, as applied to claim 33 above, Hossian discloses all the limitations include, the metal layer is silicided and metal layer is selected form platinum tungsten tantalum palladium or nickel and silicided on source and drain to form electrodes(Column 9, lines 20-45)

Pertaining claim 38, as applied to claim 33, Hossian discloses all the limitations include, source and drain electrodes are formed from rare earth silicides (Column 9, lines 20-45, rare earth material tantalum palladium platinum)

Pertaining claim 40, as applied to claim 33 above, Hossain discloses all the limitations include, the insulation layer is formed from an oxy-nitride stack (column 6 lines 51-53, silicon oxynitride 12 is considered as oxide-nitride stack because oxide layer is formed between the nitride and the substrate).

Pertaining claim 41, as applied to claim 33 above, Hossain discloses all the limitations include, the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel (Fig.11, 46)

Pertaining claim 42, as applied to claim 33 above, Hossain discloses all the limitations include, an entire interface between a least on of the source and drain electrode and the semiconductor substrate formed a Schottky contact or Schottky-like region with the semiconductor substrate.(Fig. 11, silicide layer 46 covers all source and drain region 30)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4,10,12, 15-32, 39,& 44-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hossain et al. (US 6242785) in view of Wallace et al.(US 6013553)

Pertaining claims 4 & 10, as applied to claims 1, 2 or 3 above paragraph 3, Hossain discloses all the limitations include, the gate insulation layer (Fig. 13, 12)

However, Hossain fails to teach the gate insulation layer is formed from metal oxide.

Wallace discloses the gate insulation layer is formed form hafnium oxynitride (Fig. 8, zirconium (or hafnium) oxynitride 36 is gate insulating layer)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention is made to provide Hossain with metal oxide gate insulating layer taught by Wallace in order to produce reliable device (Column 2 lines 54-57).

Pertaining claim 12, as applied to claim 10 above paragraph 5, Hossian and Wallace in combination discloses all the limitations include, the Schottky contact or Schottky-like region (See Hossian, Fig 13, 46) is formed at least in area adjacent to the channel and wherein dopant are introduced into to channel region(See Hossain, Fig. 1, 18).

Pertaining claims 15 & 24, Hossain discloses a method for manufacturing of a device for regulating the flow of electrical current, the method comprising;

provide for a semiconductor substrate (Fig. 1, 10);

providing for an electrical insulating layer in contact with the semiconductor substrate (Fig. 10, silicon oxynitride 12 has dielectric constant from 3.8 to 7.5 depended on content of oxygen and nitrogen)

providing for a gate electrode (Fig. 12, 38 source and drain electrode) in contact with at least with the semiconductor substrate and proximal to the gate electrode(Fig. 12, 14) wherein at least one of the source electrode and the drain electrode (Fig. 12, source and drain 30) forms a Schottky contact or Schottky-like region(Fig. 9-13, column 9 lines 20-45, a metal layer (40) selected from platinum tungsten tantalum palladium or nickel and silicided on source and drain to form electrodes) with the semiconductor substrate(Fig. 12, 38)

Hossain fails to discloses gate insulating layer has dielectric constant greater than 7.6 in claim 15 or 15 in claim 24

However, Wallace discloses gate insulating layer (Fig. 8, zirconium (or hafnium) oxynitride 36 is gate insulating layer) has dielectric constant around 15 –30.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention is made to provide Hossain with gate insulating layer has high k dielectric constant taught by Wallace in order to produce reliable device (Column 2 lines 54-57).

Pertaining claims 16 & 25, as applied to claims 15 & 24 above paragraph 5, Hossain and Wallace in combination discloses all the limitations include, the metal layer is silicided and metal layer is selected form platinum tungsten tantalum palladium or nickel and silicided on source and drain to form electrodes (Column 9, lines 20-45)

Pertaining claims 17 & 26, as applied to claims 15 & 24 above paragraph 5, Hossain and Wallace in combination discloses all the limitations include, source and drain electrodes are formed from rare earth silicides (Column 9, lines 20-45, rare earth material tantalum palladium platinum)

Pertaining claims 18 & 27, as applied to claims 15 & 24 above paragraph 5, Hossain and Wallace discloses all the limitations include, the gate insulation layer is formed form hafnium oxynitride (Wallace, Fig. 8, zirconium (or hafnium) oxynitride 36 is gate insulating layer)

Pertaining claims 19 & 28, as applied to claims 15 & 24 above paragraph 5, Hossain and Wallace discloses all the limitations include, the insulation layer is formed from an oxy-nitride stack (Hossain, column 6 lines 51-53, silicon oxynitride 12 is considered as oxide-nitride stack because oxide layer is formed between the nitride and the substrate).

Pertaining claims 20 & 29, as applied to claims 10 & 24 above paragraph 5, Hossian and Wallace in combination discloses all the limitations include, the Schottky contact or Schottky-like region (See Hossian, Fig 13, 46) is formed at least in area adjacent to the channel and wherein dopant are introduced into to channel region(See Hossain, Fig. 6, 28).

Pertaining claims 21 & 30, as applied to claims 15 & 24 above paragraph 5, Hossain and Wallace discloses all the limitations include, an entire interface between a least on of the source and drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.(Hossain, Fig. 11, silicide layer 46 covers all source and drain region 30)

Pertaining claims 22 & 32, as applied to claims 15 & 24 above paragraph 5, Hossain discloses all the limitations include, include, the insulation layer is more than one layer (Hossian, Fig. 13, 12, Oxide layer and nitride layer become oxynitride layer)

Pertaining claims 23 & 31, as applied to claims 15 & 24 above, Hossain and Wallace discloses all the limitations include, dopant are introduced into the channel region (Hossain, Fig. 1, 18)

Pertaining claim 39, as applied to claim 33 above paragraph 3, Hossain discloses all the limitations include, the gate insulation layer (Fig. 13, 12)

However, Hossain fails to teach the gate insulation layer is formed from metal oxide.

Wallace discloses the gate insulation layer is formed form hafnium oxynitride (Fig. 8, zirconium (or hafnium) oxynitride 36 is gate insulating layer)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention is made to provide Hossain with metal oxide gate insulating layer taught by Wallace in order to produce reliable device (Column 2 lines 54-57).

Pertaining claims 44 & 55, Hossian discloses a method for manufacture of device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate(Fig. 1, 10);

providing for an electrically insulating layer in contact with the semiconductor substrate the insulating layer having a dielectric constant (Fig. 6, silicon oxynitride 12 having dielectric constant from 3.5 to 7.5)

providing for a gate electrode located in contact with at least a portion of the insulating layer(Fig. 6, 12)

exposing the semiconductor substrate one or more areas proximal to the gate electrode(Fig. 6, source and drain region have been exposed by etching gate insulating layer 12);

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate(Fig. 10, 40);

reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate(Fig. 13, 46).

Hossain fails to discloses gate insulating layer has dielectric constant greater than 7.6 in claim 44 or 15 in claim 55

However, Wallace discloses gate insulating layer (Fig. 8, zirconium (or hafnium) oxynitride 36 is gate insulating layer) has dielectric constant around 15 –30.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention is made to provide Hossain with gate insulating

layer has high k dielectric constant taught by Wallace in order to produce reliable device (Column 2 lines 54-57).

Pertaining claims 45 & 56, as applied to claims 44 & 55 above paragraph 3, Hossian and Wallace in combination disclose all the limitations include, deposition a thin conducting film on the insulating layer (Hossian, Fig.9-11, 40);

patterning and etching the conducting film to form a gate electrode (Hossian, Fig. 11, patterned and etching the conducting film 40 on sidewalls portion etched out);

forming one or more thin insulating layers(Hossian, Fig. 12, 22) on one or more sidewalls of the gate electrode (Hossian, Fig. 12, 14)

Pertaining claims 46 & 57, as applied to claims 44 & 55 above paragraph 5, Hossian and Wallace in combination disclose all the limitations include, removing metal not reacted during the reacting process (Hossian, Fig. 10-11, metal not reacted during the thermal process has been removed on side spacer (Fig. 11, 22) region)

Pertaining claims 47 & 58, as applied to claims 44 & 55 above paragraph 5, Hossian and Wallace in combination disclose all the limitations include, the thermal annealing process (Hossian, column 9, lines 29-31 "thermal process includes heating substrate to a temperature greater than 600 °C")

Pertaining claims 48 & 59, as applied to claims 44 & 55, Hossian and Wallace in combination disclose all the limitations includes, the metal layer is silicided and metal layer is selected form platinum tungsten tantalum palladium or nickel and silicided on source and drain to form electrodes (Column 9, lines 20-45)

Pertaining claims 49 & 60, as applied to claims 44 & 55 above paragraph 5, Hossian and Wallace in combination disclose all the limitations include, source and drain electrodes are formed from rare earth silicides (Hossian, column 9, lines 20-45, rare earth material tantalum palladium platinum)

Pertaining claims 50 & 61, as applied to claims 44 & 55 above paragraph 5, Hossian and Wallace in combination disclose all the limitations include, the gate insulation layer is formed form metal oxide (Wallace, Fig. 8, zirconium (or hafnium) oxynitride 36 is gate insulating layer)

Pertaining claims 51 & 62, as applied to claims 44 & 55 above paragraph 5, Hossian and Wallace in combination disclose all the limitations include, the insulation layer is formed from an oxy-nitride stack (column 6 lines 51-53, silicon oxynitride 12 is considered as oxide-nitride stack because oxide layer is formed between the nitride and the substrate).

Pertaining claims 52 & 63, as applied to claims 44 & 55, Hossian and Wallace in combination disclose all the limitations includes, the Schottky contact or Schottky-like region (See Hossian, Fig 13, 46) is formed at least in area adjacent to the channel and wherein dopant are introduced into to channel region (See Hossain, Fig. 6, 28).

Pertaining claims 53 & 64, as applied to claims 44 & 55 above paragraph 5, Hossian and Wallace in combination disclose all the limitations includes, an entire interface between a least on of the source and drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate (Hossian, Fig. 11, silicide layer 46 covers all source and drain region 30)

Pertaining claims 54 & 65, as applied to claims 44 & 55 above paragraph 5, Hossian and Wallace in combination disclose all the limitations includes, dopant are introduced into to channel region (See Hossain, Fig. 6, 28).

Response to Arguments

Applicant's arguments filed 3/21/2007 have been fully considered but they are not persuasive.

With respect to claims rejection under 35 U.S.C. 102(e), applicant argues that "Hossain fails to discloses or teach reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate"(Applicants' Remark/Argument on page 16, lines 1-2).

In response to applicant's contention, it is respectfully submitted that **Hossain et al. (US 6242785, hereafter Hossain)** discloses all the claimed limitation including "the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate" below.

Hossain appears to show, see Fig. 9, a metal with the exposed semiconductor substrate 10 (including source and drain region) such that a Schottky or Schottky-like source electrode and drain electrode are formed (column 9, lines 20-45) on the semiconductor substrate.

Also applicant argues that "As source and drain 30 are formed by ion implantation of impurities into the substrate 10, the source and drain regions 30 are

formed materially different from the substrate 10 and are no longer substrate region" (Applicants' Remark/Argument on page 16, lines 20-23).

In response to applicant's contention, applicant claims - - "at least one of the source electrode and the drain electrode forms a Schottky-contact or Schottky-like region with the semiconductor substrate" as recited in claim 1. However, Applicant did not claim materially different or same in the claim language.

Furthermore, "a substrate," has no special meaning in the claims other than any silicon containing material including a source and drain because applicant has not defined that such meaning entails or define.

"Claim terms are presumed to have the ordinary and customary meanings attributed to them by those of ordinary skill in the art.

Therefore, the rejection of claims 1-3, 5-11,13,14,33-38, and 40-42 under 35 U.S.C. 102(e) is deemed proper.

In addition, for the rejection of claims 4,10,12,15-32,29, and 44-64, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Su C. Kim whose telephone number is (571) 272-5972. The examiner can normally be reached on Monday - Thursday, 9:00AM to 7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Su C Kim

W. David Coleman
Primary Examiner